IN THE CLAIMS:

Claims 1, 5, 12, 15, 21, 26, 30, 33, 37 and 40 have been amended, as follows:

1. (currently amended) A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals;

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays; and

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows of the at least one memory are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation.

2. (Original) The method of claim 1, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

3. (cancelled).

4. (cancelled).

5. (Currently Amended) A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals; and

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, wherein multiple rows [[per]] of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command.

6. (Original) The method of claim 1, wherein the method is performed using a synchronous dynamic random access memory device.

7. (Original) The method of claim 3, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

8. (currently amended) An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals;

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays; and

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows [[per]] of the least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation.

9. (Original) The article according to claim 8, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

10. (Cancelled)

11. (Cancelled)

12. (currently amended) An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals; and

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, wherein multiple rows [[per]] of at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command.

13. (Original) The article according to claim 8, wherein the method is performed using a synchronous dynamic random access memory device.

14. (Original) The article according to claim 10, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

15. (currently amended) A memory device responsive to command signals and bank address signals, the memory device comprising:

multiple memory bank arrays, each memory bank array having storage cells; and

a command controller/decoder responsive to selected command signals and bank address signals to initiate an auto-refresh command controlling an auto refresh operation to at least one specified memory bank array of the multiple memory bank arrays, and before or during the auto refresh operation to the at least one of the specified memory bank arrays, issue a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows [[per]] of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation.

16. (Original) The memory device of claim 15, wherein the at least one specified memory bank array of the multiple memory bank arrays is determined based on which memory bank arrays have been refreshed and a subsequent known order of refreshing the memory bank arrays.

17. (Original) The memory device of claim 16, wherein the at least one specified memory bank array of the multiple memory bank arrays is determined based on a command specifying which bank is to be next refreshed and a subsequent known order of refreshing the memory bank arrays.

18. (Cancelled)

19. (Original) The memory device of claim 15, further comprising a refresh counter for incrementing an address of a row to be refreshed, wherein the refresh counter has a separate counter portion for each of the multiple memory bank arrays.

20. (Cancelled)

21. (currently amended) A memory device responsive to command signals and bank address signals, the memory device comprising:

multiple memory bank arrays, each memory bank array having storage cells; and

a command controller/decoder responsive to selected command signals and bank address signals to initiate an auto-refresh command controlling an auto refresh operation to at least one specified memory bank array of the multiple memory bank arrays, wherein multiple rows [[per]] of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command.

22. (Original) The memory device of claim 15, wherein the memory device is a synchronous dynamic random access memory.

23. (Previously Presented) The memory device of claim 15, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

24. (Cancelled)

25. (Previously Presented) The method of claim 26, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

26. (currently amended) A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals;

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays; and

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows [[per]] of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command.

27. (Previously Presented) The method of claim 26, wherein the method is performed using a synchronous dynamic random access memory device.

28. (Previously Presented) The method of claim 26, wherein the second operation is selected from the group consisting of activate operations, read operations,

write operations and precharge operations.

29. (Original) The method of claim 28, wherein second command signals, to initiate an activate operation to open a page not to be refreshed, are issued by the memory controller after first command signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page.

30. (currently amended) A memory controller for controlling a memory device having multiple memory bank arrays comprising:

a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, and the second command signals initiate, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows [[per]] <u>of the at least one</u> memory bank array are refreshed in a staggered fashion <u>relative to other rows in the memory bank array</u> per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation.

31. (Original) The memory controller of claim 30, wherein the specified at

least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

32. (Cancelled)

33. (currently amended) A memory controller for controlling a memory device having multiple memory bank arrays comprising:

a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, and the second command signals initiate, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows [[per]] of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the auto-refresh command.

34. (Original) The memory controller of claim 30, wherein the memory device is a synchronous dynamic random access memory device.

35. (Original) The memory controller of claim 30, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

36. (Original) The memory controller of claim 35, wherein second

command signals to initiate a second activate operation to open a page not to be refreshed are issued by the memory controller after first command signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page.

37. (currently amended) A system comprising:

a memory device having multiple memory bank arrays; and

a memory controller for controlling the memory device, including a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, and the second command signals initiate, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows [[per]] <u>of the at least one</u> memory bank array are refreshed in a staggered fashion <u>relative to other rows in the memory bank array</u> per the auto-refresh command and the second operation begins after all the rows have begun the auto refresh operation.

38. (Original) The system of claim 37, wherein the specified at least one of

the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

39. (Cancelled)

40. (currently amended) A system comprising:

a memory device having multiple memory bank arrays; and

a memory controller for controlling the memory device, including a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, and the second command signals initiate, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, wherein multiple rows [[per]] of the at least one memory bank array are refreshed in a staggered fashion relative to other rows in the memory bank array per the auto-refresh command.

41. (Original) The system of claim 37, wherein the memory device is a synchronous dynamic random access memory device.

42. (Original) The system of claim 37, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

43. (Original) The system of claim 42, wherein second command signals to initiate a second activate operation to open a page not to be refreshed are issued by the memory controller after first command signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page.